Exploiting Fixed Charge to Control Schottky Barrier Height in $Si|AlO_x|MoO_x$ – based Tunnel Diodes

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Introduction

Carrier selective contacts have become one of the leading advancements in photovoltaics with the most efficient structures exceeding 26% conversion efficiency [1]. Carrier selectivity increases the efficiency and cost effectiveness of solar cells by reducing recombination at metal contacts and avoiding highly doped emitter layers. Popular selective contact materials are often transition metal oxides (TMOs) [2,3]. In contrast to previous articles, recent studies have indicated that the interface of p-type silicon and molybdenum oxide (MoO_x) exhibits a significant Schottky barrier (Φ_{bh}) that decreases the efficiency of hole-selective contacts by impeding majority carrier hole collection.

To alleviate this issue, the current work utilizes atomic layer deposited (ALD) alumina (AlO_x) between Si wafer and MoO_x with the expectation to generate a negative interface fixed charge (N_f) after annealing, decreasing band bending and increasing hole selectivity [1,4]. ALD AlO_x also provides passivation to decrease interface trap state density (D_{it}) with diffusion of precursor hydrogen during annealing [5-7].

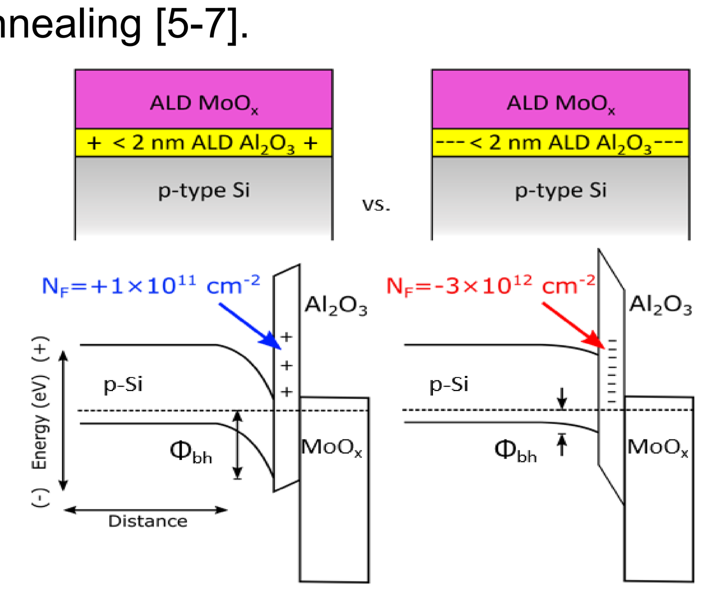
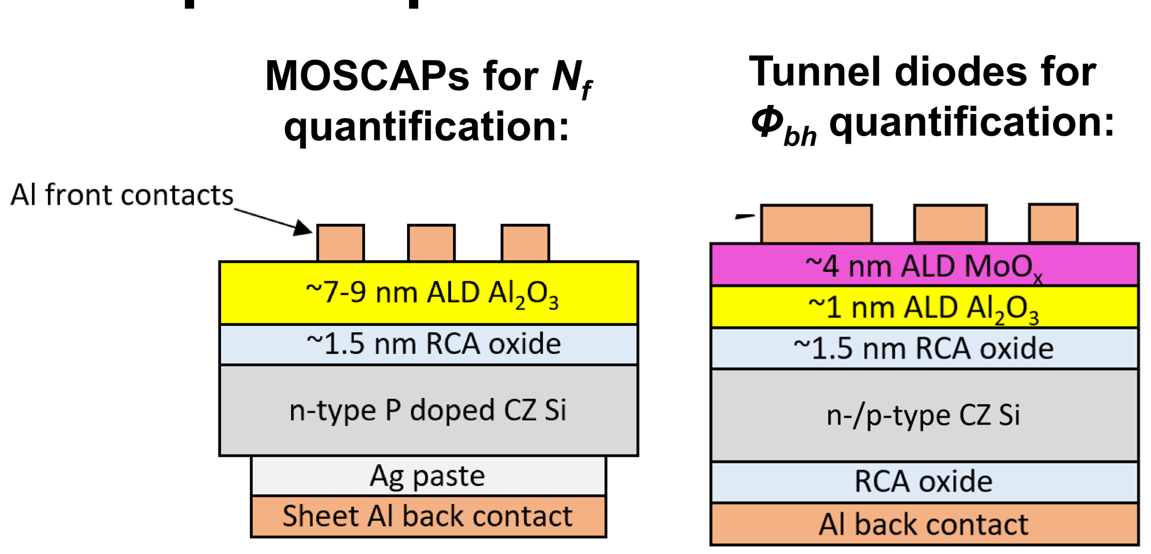


Figure 1. Schematic of tunnel diode structures with as deposited (left) and annealed (right) Al_2O_3 and respective band diagrams.

Sample Preparation

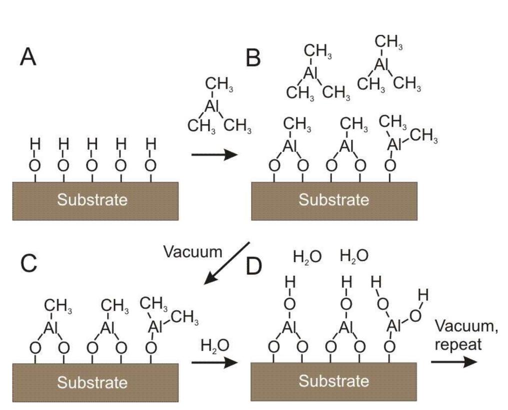


Si surface preparation:

- SC-1, SC-2 (RCA-terminated)

Atomic layer deposition (ALD):

- Al_2O_3 : *Trimethylaluminum (TMA) and H_2O at 80-300°C*
- MoO_x : *Bis(tert-butylimido)bis(dimethylamido) Mo and O_3 at 200°C*



MOSCAP electrical analysis

N_f from capacitance-voltage (C – V)

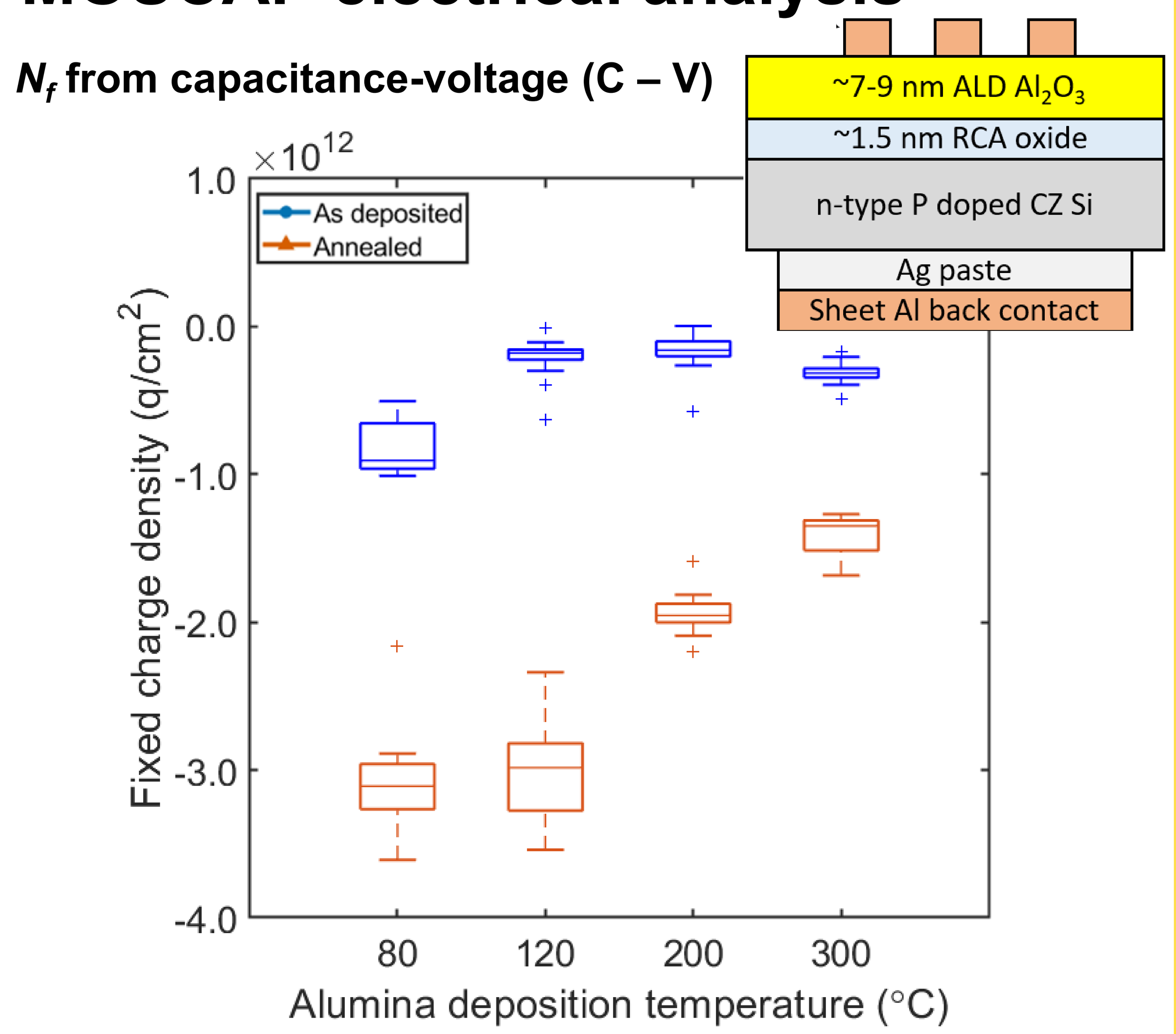


Figure 2. Fixed charge density of $n\text{-}Si|Al_2O_3|Al$ capacitors as-deposited and annealed at 425°C for 20 min in N_2. [8]

- As-deposited samples have less negative N_f compared to annealed samples, with lower deposition temperature annealed samples having largest $|N_f|$.

D_{it} - Terman method (C – V)

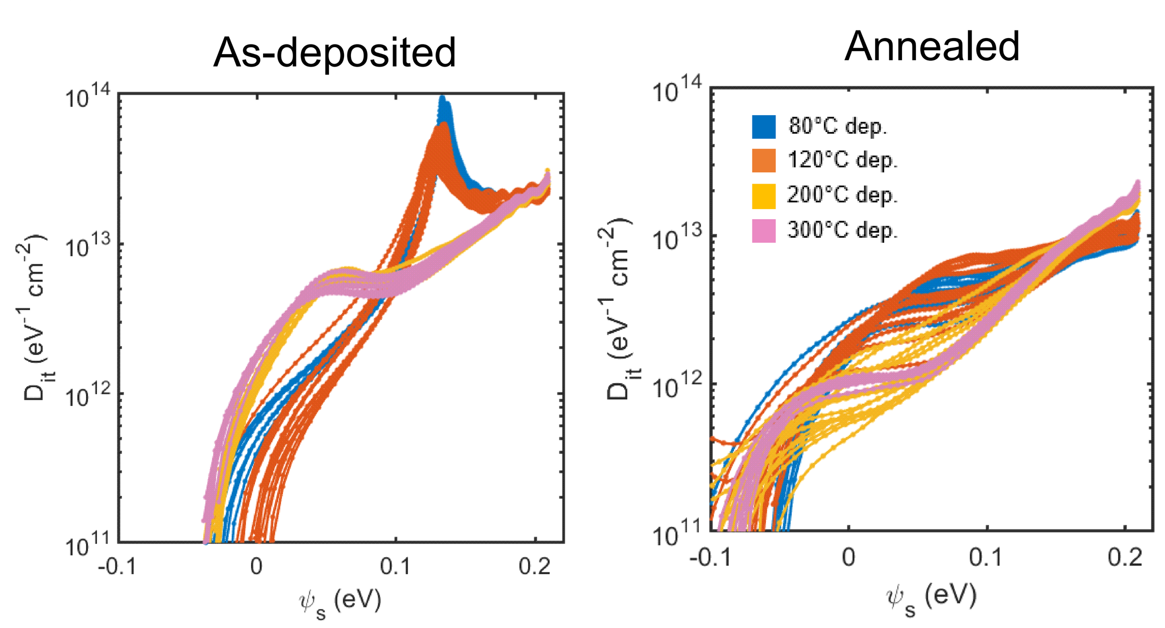


Figure 3. Terman method density of interface trap state density as a function of potential (φ_s) for $n\text{-}Si|Al_2O_3|Al$ capacitors.[8]

D_{it} - Conductance method (G – F)

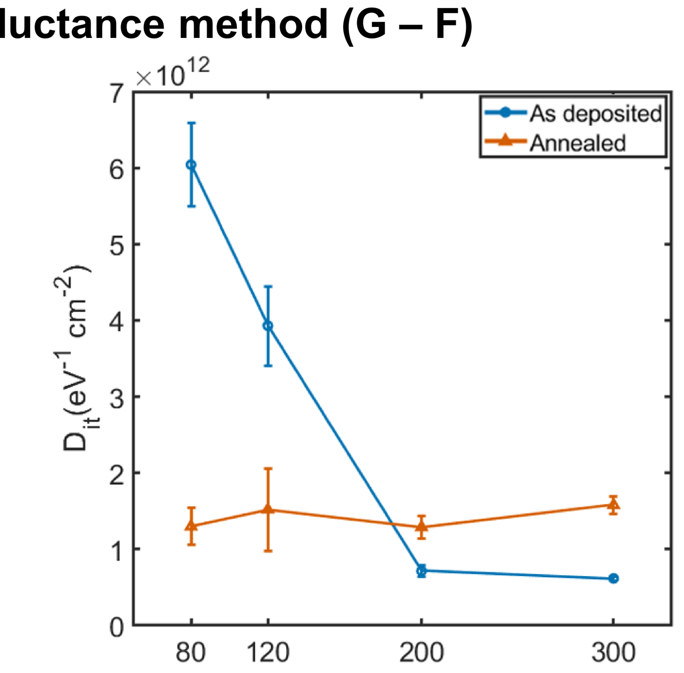


Figure 4. Density of interface traps as determined using the conductance method at flat band voltage as a function of deposition temperature. [8]

- Annealed samples in general have a lower D_{it} than as-deposited at depositions < 200°C for both methods.

Tunnel diode electrical analysis

Current density-voltage (J – V) diode rectification

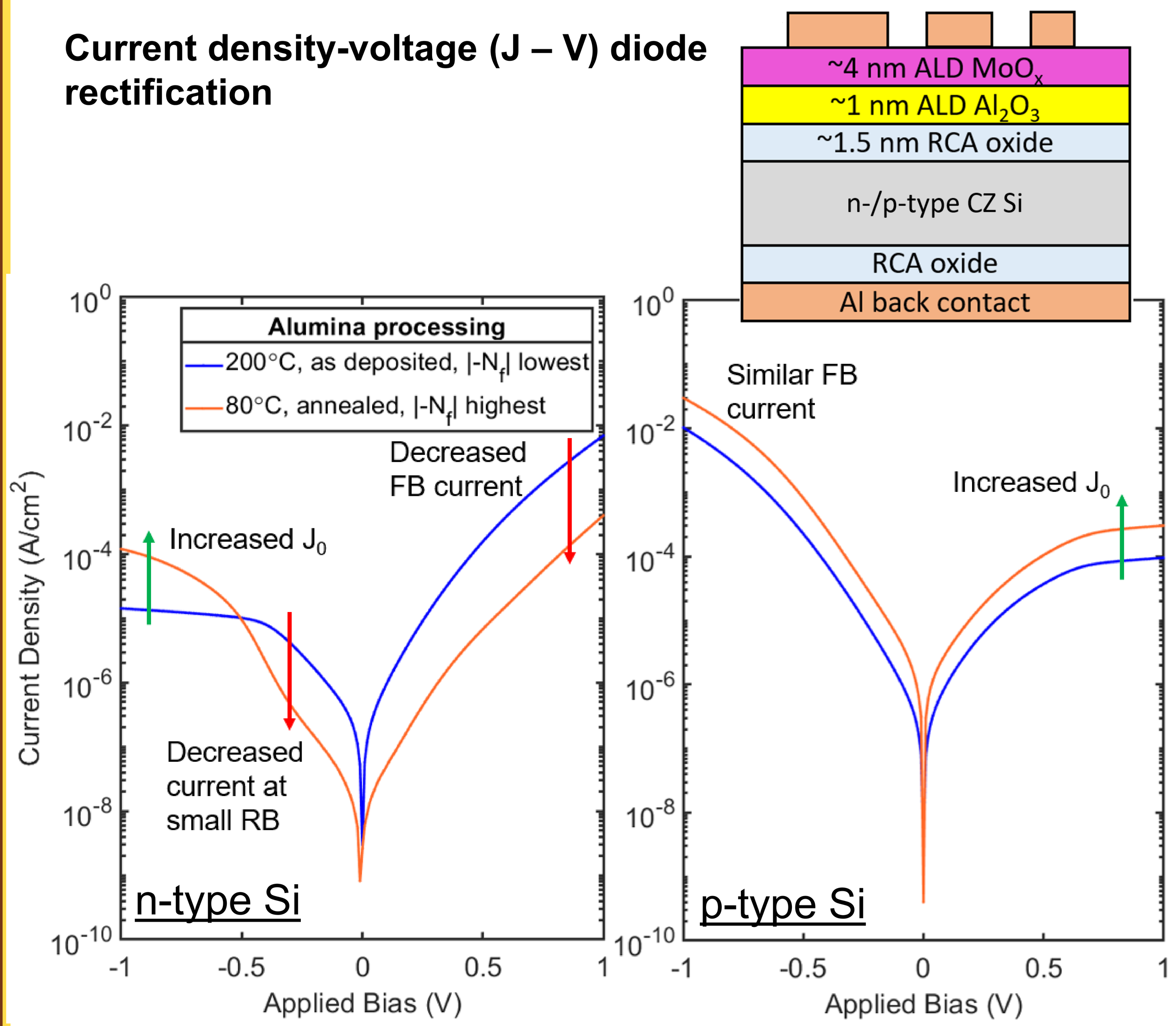


Figure 5. Room temperature J-V data for $n/p\text{-}Si|Al_2O_3|MoO_x|Al$ samples with the lowest and highest expected magnitude of N_f.

- n- and p-type Si tunnel diodes exhibited opposite trends in current density with alumina processing, aside from n-type at high reverse bias.
    - Possibly coincides with $|N_f|$ changes from C – V measurements, though Rs was found to be high.

Mott-Schottky ($1/C^2$ – V)

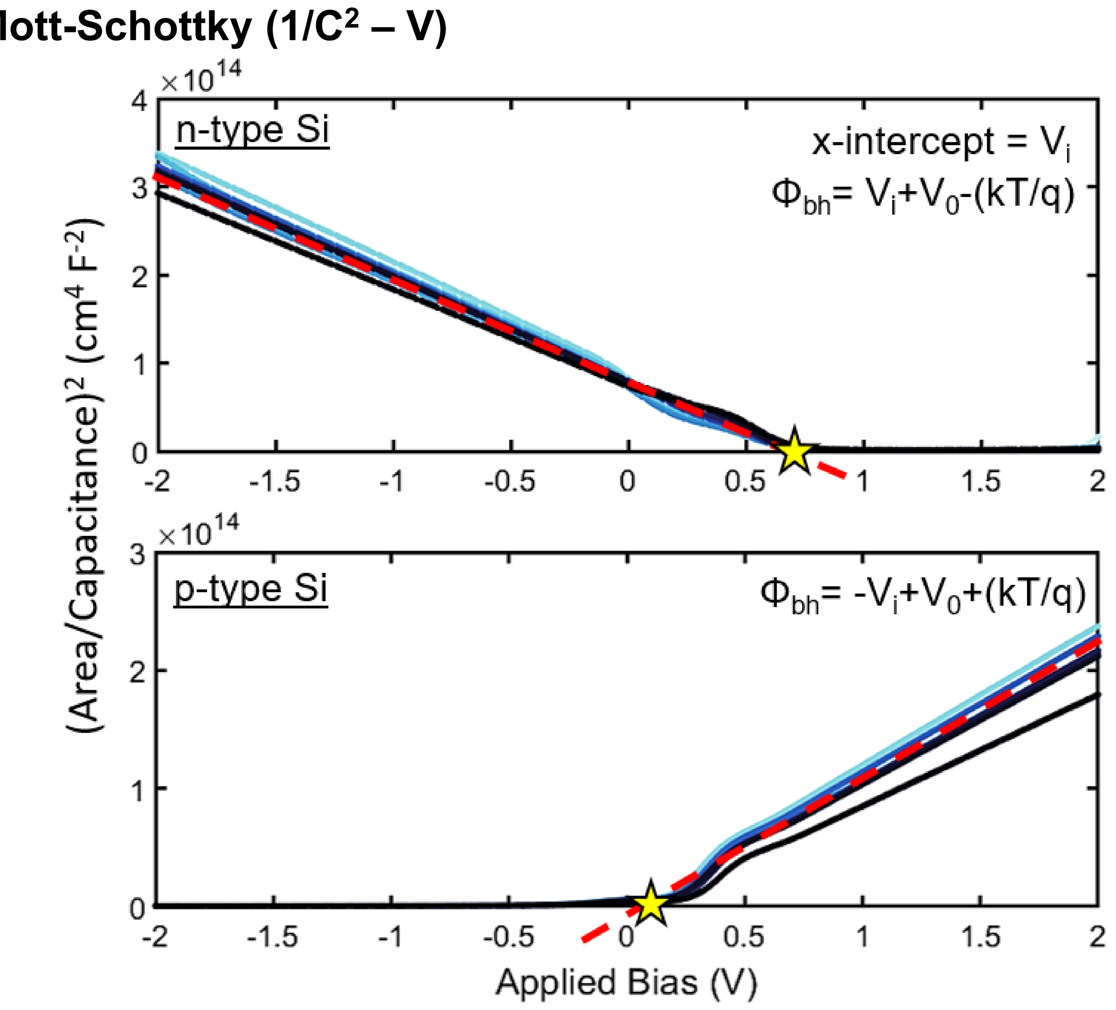


Figure 6. Example plot of area²/C²-V for all contact pads on $n/p\text{-}Si|Al_2O_3|MoO_x|Al$ samples with alumina deposited at 200°C.

- Capacitance-voltage (C-V) measurements conducted at high frequency (100 kHz)
- Φ_{bh} extrapolated from plotting $(A/C)^2$ as a function of voltage [8].

Tunnel diode Φ_{bh} summary

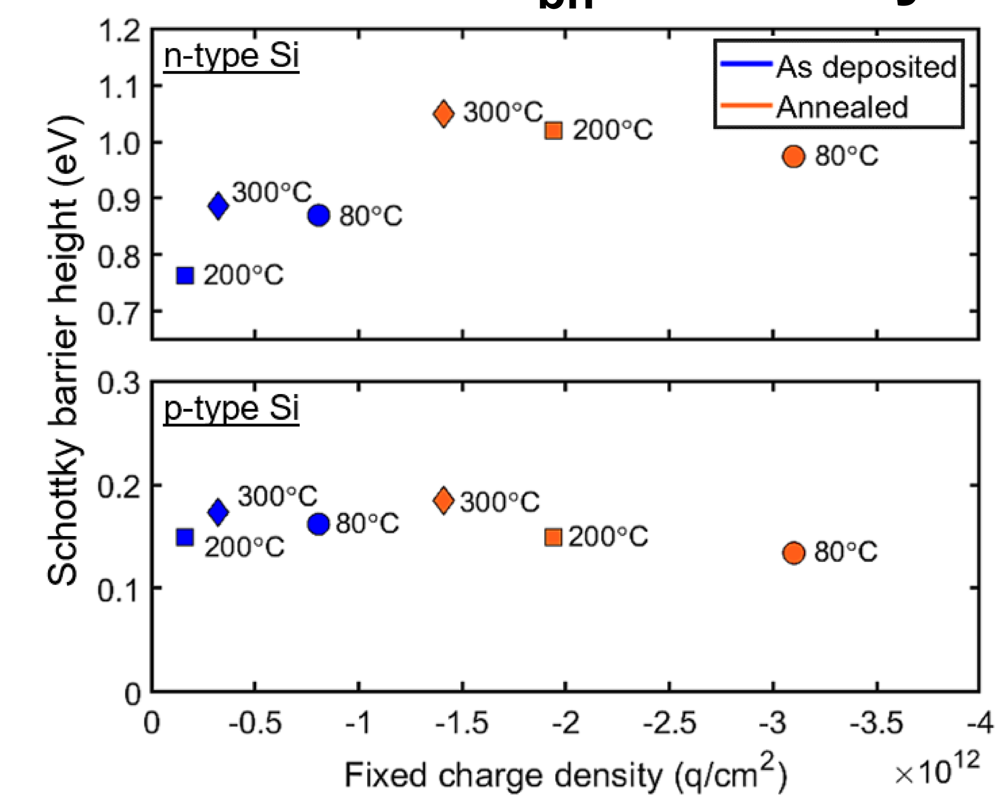


Figure 7. Average Φ_{bh} calculated from Mott-Schottky analysis plotted against fixed charge density for $n/p\text{-}Si|Al_2O_3|MoO_x|Al$ with different processing conditions.

Conclusions

- Φ_{bh} is dependent on a negative N_f and is shown to be controlled with processing
- n-type Si barrier height can be increased
- Effect in p-type Si remains inconclusive
    - May be too small to measure by Mott-Schottky method.

References

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Acknowledgements

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